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10/583,868	06/21/2006	Tetsuya Hirano	292813US2PCT	8990

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/583,868	HIRANO, TETSUYA	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/21/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/21/2006 and 3/20/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/583,868 has a total of 6 claims pending in the application, there are 4 independent claims and 2 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on application JP 2003-423963 and JP 2003-423964 filed in Japan on December 22, 2003. The instant application is a national stage entry of PCT/JP04/017684, having an international filing date of November 29, 2004.

INFORMATION CONCERNING THE ABSTRACT

The abstract of the disclosure is objected to because of the term "DPS" is used. The examiner believes "DSP" is meant instead. Correction is required. See MPEP § 608.01(b).

INFORMATION CONCERNING DRAWINGS

The applicant's drawings submitted 6/21/2006 are acceptable for examination purposes.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P. ' 609 (C)**, the applicant's submission of the Information Disclosure Statement, dated March 20, 2007, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. ' 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Regarding the information disclosure statement filed June 21, 2006, the document fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. Of the references listed, only JP 11-167517 has been considered. The other references have been placed in the application file, but the information referred to therein has not been considered.

CLAIM OBJECTIONS

Claims 1, 2, 4 and 6 are objected to because of the following informalities: grammatical errors: “at lease two bus cycles” (has been interpreted “at least two bus cycles”); "the DSP is accessing to the external memory” (has been interpreted “the DSP is accessing the external memory”.

Claims 3-6 are objected to because of the following informalities in Claims 3 and 5: grammatical errors: "at the same timing" (interpreted "at the same time"); "allowed to perform memory access" (interpreted as "allowed to perform the memory access"); "acquires a data" (has been interpreted as "acquires data"); "outputting a data" (interpreted as "outputting data"). Also, Claim 6 has the phrase "dose not access" (interpreted as "does not access").

Regarding Claims 5, the language "issues a read command or a write command in the timing" is believed to have been "issues a read command or a write command at the same time".

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC ' 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 4 and 6 use the phrase "plural commands." What a plural command is has not been made clear in the specification, nor do the respective DSPs seem able to issue multiple simultaneous ('plural') commands. The

language has been construed to mean the DSPs are both issuing commands at the same time.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kutaragi et al (US 5,111,530).

Regarding Claim 1, Kutaragi teaches a data processor comprising, at least, a CPU for controlling an entire system (CPU 13 in Figure 4), a DSP for performing preset processing (Signal Processor 11 in Figure 4), and an external memory to be accessed by the DSP and to be capable of being accessed through the DSP by the CPU (External RAM 14, the host must go through the DSP to access the RAM);

the DSP being configured to have at least two bus cycles as a unit of one data access (Figure 12E, where the DSP is taking two bus cycles to access a unit of data), the number of the bus cycles used in the unit of one data access being selectable (the amount of cycles dedicated to accessing a unit of data from the memory by the DSP is adjustable as described in Column 16 Lines 28-45, note particularly how the 'access

periods can be properly adjusted' on Lines 31-32), and a data length to be accessed to the external memory being variable (time-division control circuit 94 [in Figure 10] can adjust how long the DSP accesses the memory for, Column 16 Lines 28-34);

the DSP including:

a determination means for determining whether the DSP is accessing the external memory or not (the determination means corresponds to time-division control circuit 94 of Figure 10, since it determines whether the DSP or CPU is accessing the external memory, Column 16 Lines 34-45);

a control means for determining whether the CPU is allowed to access the external memory, based on the presence and absence of a signal from a determination means (time-division control circuit 94 also acts as a control means, as it determines which device is allowed to access the memory, Column 16 Lines 34-45, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data); and

means for performing a switching operation of an address and a data in connection with the external memory according to a command from the control means, and inputting or outputting the address and the data based on the switching operation (Figure 10, the latches 97-99 switch connections of the address and data signals depending on which device the time-division control circuit decides is accessing the external memory, Column 16 Lines 38-45);

wherein in a case where the data length is selected so as to perform accessing by a maximum number of bus cycles, when the determination means determines that

the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control means (Column 16 Lines 28-58, the time-division control circuit can adjust the memory bus to be accessed the DSP only, thus the CPU is not allowed to access the memory, placing the CPU in a wait state, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data), and in a case where the data length is not selected so as to perform accessing by a maximum number of the bus cycles, the control means allows the CPU to access the external memory by utilizing a free bus cycle (see for example, Figure 12D and Figure 12E, the last bus cycle is used by the CPU to access the external memory).

Regarding Claim 2, Kutaragi teaches a data processor comprising, at least, a CPU for controlling an entire system (CPU 13), a sound source for supplying a musical tone signal (ROM 1, Column 4 Lines 55-68), a DSP for performing preset processing to apply a desired effect to the musical tone signal supplied from the sound source (DSP 11, also see effects processing description on Column 3 Lines 24-27), and an external memory to be accessed by the DSP and to be capable of being accessed through the DSP by the CPU (External RAM 14, the host must go through the DSP to access the RAM);

the DSP being configured to have at least two bus cycles as a unit of one data access with respect to processing of the musical tone signal (Figure 12D, where the DSP is taking two bus cycles to access a unit of data), the number of the bus cycles

used in the unit of one data access being selectable (the amount of cycles dedicated to accessing a unit of data from the memory by the DSP is adjustable as described in Column 16 Lines 28-45, note particularly how the 'access periods can be properly adjusted' on Lines 31-32), and a data length to be accessed to the external memory being variable (time-division control circuit 94 [in Figure 10] can adjust how long the DSP accesses the memory for, Column 16 Lines 28-34);

the DSP including:

a determination means for determining whether the DSP is accessing the external memory or not (the determination means corresponds to time-division control circuit 94 of Figure 10, since it determines whether the DSP or CPU is accessing the external memory, Column 16 Lines 34-45);

a control means for determining whether the CPU is allowed to access the external memory, based on the presence and absence of a signal from a determination means (time-division control circuit 94 also acts as a control means, as it determines which device is allowed to access the memory, Column 16 Lines 34-45, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data); and

means for performing a switching operation of an address and a data in connection with the external memory according to a command from the control means, and inputting or outputting the address and the data based on the switching operation (Figure 10, the latches 97-99 switch connections of the address and data signals

depending on which device the time-division control circuit decides is accessing the external memory, Column 16 Lines 38-45);

wherein in a case where the data length is selected so as to perform accessing by a maximum number of bus cycles, when the determination means determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control means (Column 16 Lines 28-58, the time-division control circuit can adjust the memory bus to be accessed the DSP only, thus the CPU is not allowed to access the memory, placing the CPU in a wait state, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data), and in a case where the data length is not selected so as to perform accessing by a maximum number of the bus cycles, the control means allows the CPU to access the external memory by utilizing a free bus cycle (see for example, Figure 12D and Figure 12E, the last bus cycle is used by the CPU to access the external memory).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kutaragi in view of Davis et al (US 4,991,169).

Regarding Claim 5, Kutaragi teaches a data processor having a fixed number of memory access timings per sampling cycle (Column 16 Lines 8-11, one sampling cycle [corresponding to a machine cycle in Kutaragi] has a fixed number of memory accesses allowed, based on the timing RAM access times and length of the machine cycle) and an external memory storing musical tone waveform data (ROM 1, Column 4 Lines 55-68);

the data processor further comprising:

a first selector for outputting an address from the allowed DSP in response to a determination signal from the access determination means (switch 97 in Figure 10, note how this outputs an address from the DSP to the external memory);

However, Kutaragi does not teach multiple DSPs with a shared RAM. Davis teaches a plurality of DSPs (DSP 20 and DSP 21 in Figure 9) for accessing a single external memory in a single package (D-RAM 41 in Figure 9),

a read/write control means, which when each of the DSPs issues a read command or a write command at the same time, controls the command of which DSP is allowed (MUX 114 and controller 104 act as control means to receive signals from each DSP and Host 17, controlling which DSP is allowed to access the D-RAM, thus controlling read/writes, see Figure 9 and Column 9 Lines 30-59);

an access determination means, which when each of the DSPs issues a read command or a write command, determines which DSP is allowed to perform the

memory access (MUX 114 and controller 104 receive signals from each DSP and Host 17, controlling which DSP is allowed to access the D-RAM, thus determining which DSP has access to the memory, see Figure 9 and Column 9 Lines 30-59);

a first selector for outputting an address from the allowed DSP in response to a determination signal from the access determination means (signal C+D outputs the address from the allowed DSP, see Figure 9 and Multiplexer 114);

a second selector for outputting a data from the allowed DSP in response to the determination signal (signal A+D outputs the data from the allowed DSP, see Figure 9 and Multiplexer 142, also Column 9 Lines 9-17);

each of the DSPs including a control means for data acquisition, which acquires data from the external memory in response to the determination signal from the access determination means (each DSP can acquire data from the external memory in response to its allowed memory access, and thus has a control means to acquire data, DSP 2 through latch 126 and DSP 1 through latch 136, Column 9 Lines 4-9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have used the DSP system of Davis in the device of Kutaragi, because the shared memory of the signal processors in Davis's system allow for easy access between the processors without formal interruptions of the DSPs (Column 4 Lines 5-8 in Davis), thus increasing performance. So by combining the two devices, additional benefits are obtained.

Regarding Claim 6, Davis and Kutaragi teach the data processor according to Claim 5, wherein the read/write control means does not access the external memory

when the respective DSPs issue plural commands (see Figure 5 of Davis, where the decode and form stages of the pipeline do not involve a memory access, and since DSP 1 and DSP 2 cannot access memory at the same time, when DSP 1 is reading or writing data, DSP 2 is executing a command but is not accessing the memory).

Claim 3 is a broader version of Claim 5, and is rejected under similar rationale.

Claim 4 is a broader version of Claim 6, and is rejected under similar rationale.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:.

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-6 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

Patent Examiner
Art Unit 2185

February 15, 2008

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100